

(43) Application published **3 Sep 1987**

(21) Application No 8602998

(22) Date of filing **6 Feb 1986**

(71) Applicant
The Hymatic Engineering Company Limited

(Incorporated in United Kingdom)

**Burnt Meadow Road, North Moons Moat, Redditch,
Worcestershire B98 9HJ**

(72) Inventor
Michael Julian Richardson

(74) Agent and/or Address for Service
Kilburn & Strode,
30 John Street, London WC1N 2DD

(51) INT CL⁴
H02M 7/797

(52) Domestic classification (Edition I):

G3U 207 211 303 AA1B

**H2F 91DR 91LL 9J18 9K12 9K1 9N2A 9Q 9S1 9T2 R
U1S 2049 G3U H2F**

(56) Documents cited

GB A 2134339

GB A 2095486

EP A1 0116706

GB A 2114780

GB A 2059651

EP A2 0102614

GB A 2098369

GB 1567725

US 4424557

(58) Field of search

G3U

H2F

Selected US specifications from IPC sub-class H02P

(54) Switching bridge circuit

(57) A bridge circuit for controlling the supply of current to a load 11 from a d.c. source 13 includes four semi-conductor switches Q_1 to Q_4 each in parallel with a diode D_1 to D_4 . The voltage across the load 11 is fed back at 18 to be compared at 19 with the instantaneous value of an input wave form 12 of desired shape, and any error between the desired voltage and the actual voltage produces an error signal which controls by logic means a pulse width modulator for appropriate control of the switches Q_1 to Q_4 .

If the error is positive the circuit will alternately draw current through the load from the supply and allow the current to free wheel in the bridge circuit, whereas if the error is negative the circuit will alternately arranged for current in the load to be regenerated to the supply and to free wheel in the bridge circuit.

Fairly accurate tracking of the input wave form can be achieved. The load 11 may be a linear motor driving a reciprocating compressor.

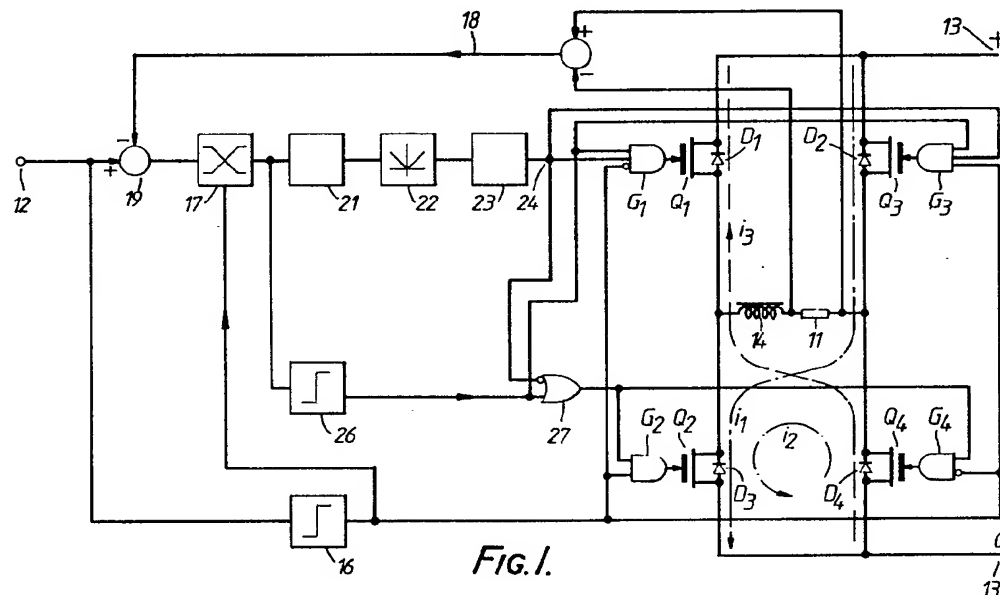


FIG. 1.

$\frac{1}{3}$ [illegible]

FIG. 1.

65B 8602978

2187312

2/3

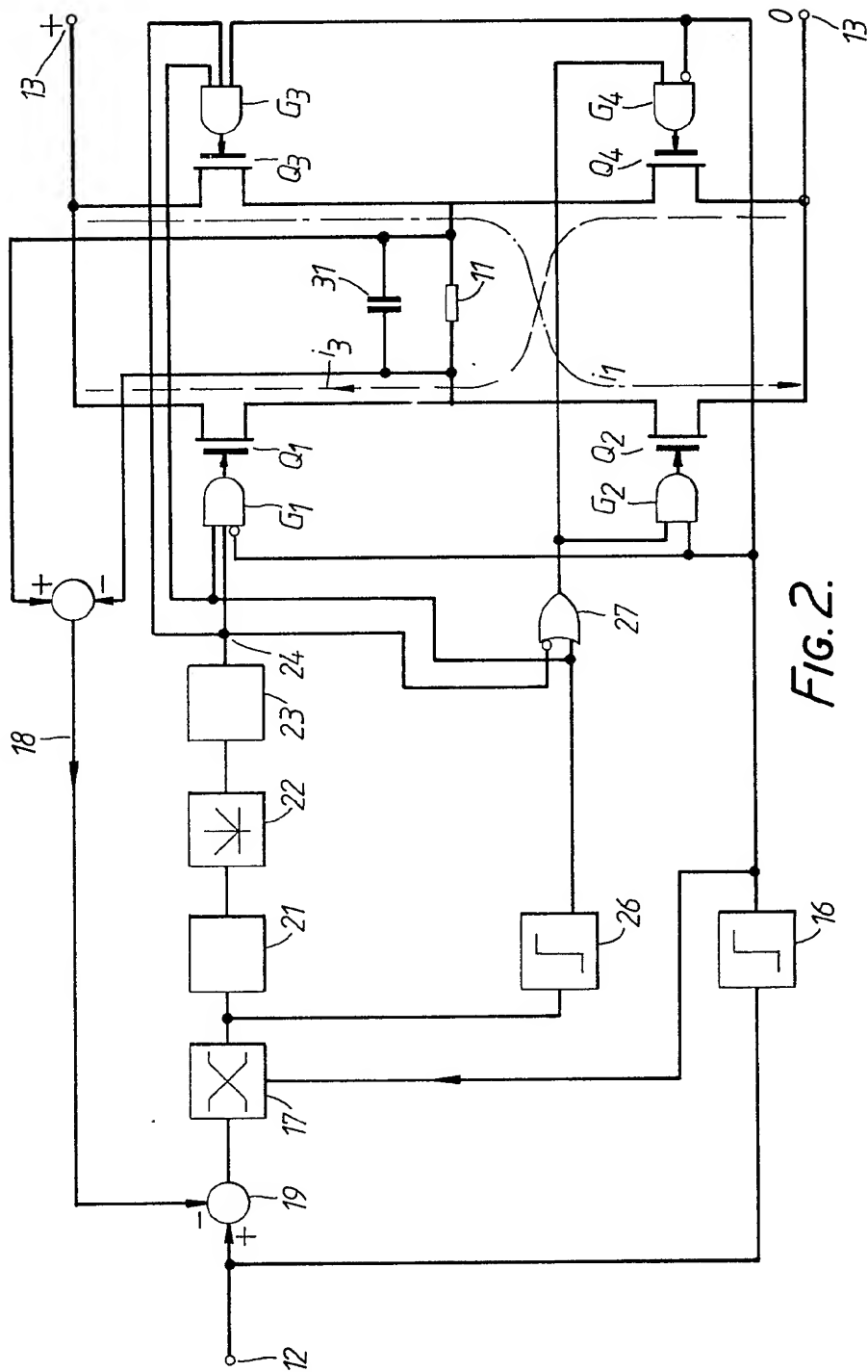
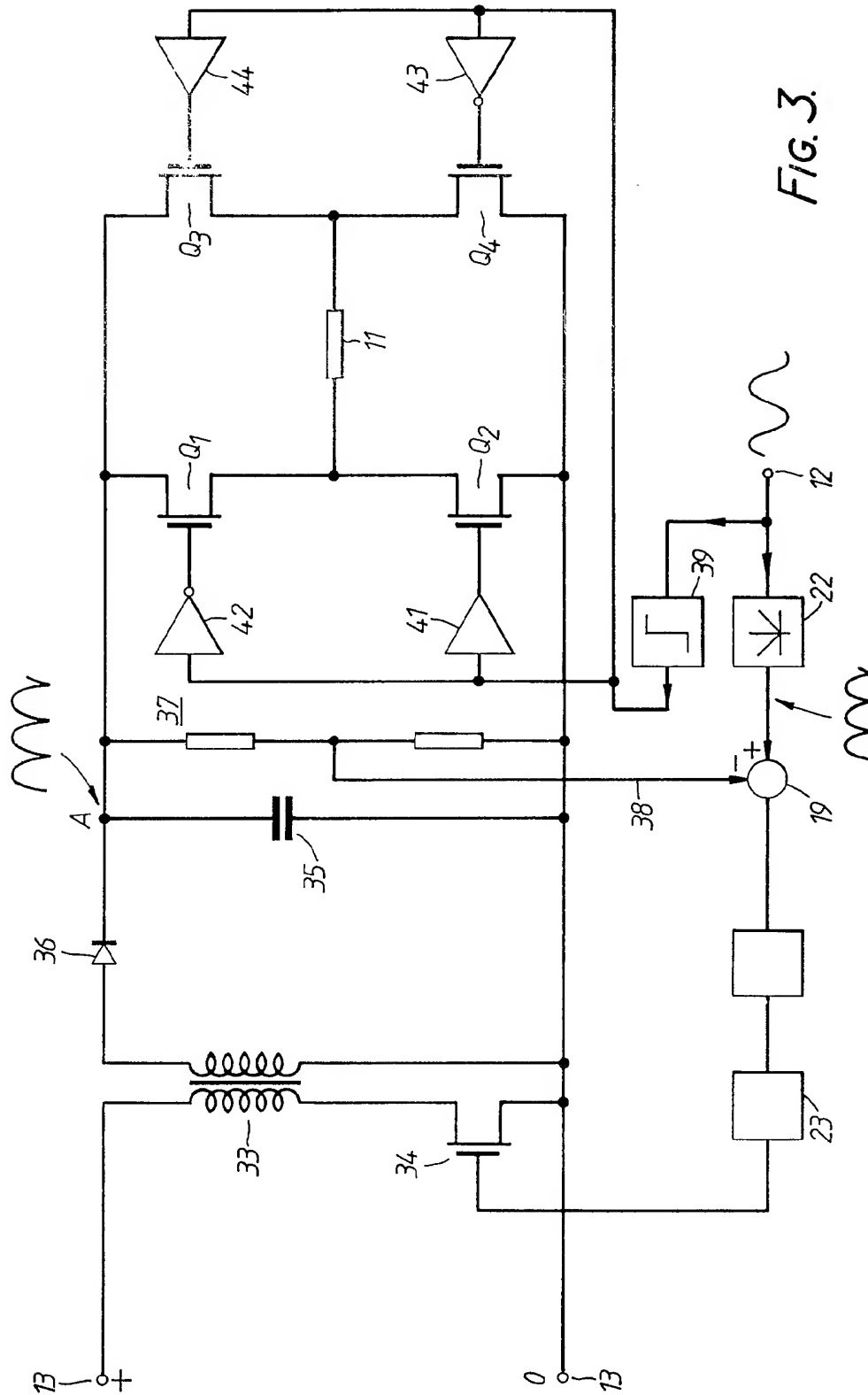


FIG. 2.

2187312

FIG. 3.



SPECIFICATION

Switching bridge circuit

5 This invention relates to switching bridge circuits for example the type of circuit in which four semiconductor switches connected in the four legs of an H are controlled by a pulse width modulating or other drive in accordance with desired characteristics to control the flow of current in a load connected in the cross bar of the H.

10 It is an object of the present invention to improve the operation of such a bridge circuit, so that the characteristics of operation of the load can accord more accurately with the desired characteristics.

15 According to the present invention a switching bridge circuit for driving a load from a d.c. supply has the switches in the bridge controlled in accordance with the desired load wave form.

20 In preferred embodiments a function of the load current or load voltage is fed back and compared with an input wave form and any resulting error signal is used to control the switches. Logic means may be arranged to operate the switches so that when the error signal has one polarity energy is fed from the load to the supply, and when the error signal has the other polarity, energy is drawn to the load from the supply.

25 It is also possible to have a mode of operation in which current in the load free wheels in the bridge circuit without drawing energy from the supply or supplying energy to the supply.

30 If the input wave form is an alternating wave form logic means may be arranged to ensure that the appropriate pair of diagonally opposite switches are used to control the load current or voltage in the respective positive and negative portions of the input wave form.

35 In a preferred embodiment of the invention pulse width modulation of the appropriate pair of diagonally opposite switches is used to control current in a load.

40 Then if the required load output is lower than the actual load output so that the error signal is positive one of the diagonal pair of switches is switched on while the other is duty cycle modulated so that the circuit alternately supplies current from the d.c. supply to the load and allows current in the load to free wheel.

45 On the other hand when the required load output is greater than the actual load output and the error is negative, one of the switches can be switched off and the other duty cycle modulated so that current in the load alternately is regenerated to the d.c. supply and allowed to free wheel.

50 According to another aspect of the invention, a switching bridge circuit for driving a load from a d.c. supply includes means for

supplying a reference signal defining a desired load wave form and feedback means for feeding back to a control circuit a signal derived from the current in, or voltage across, the load.

55 The invention may be carried into practice in various ways and three embodiments will now be described by way of example with reference to the accompanying drawings, each figure of which is a block circuit diagram of one of the embodiments of the invention.

60 Each circuit is for driving a linear motor 11 which drives a reciprocating compressor and it is desired that the load voltage closely follows the input voltage at 12 so that by providing the appropriate alternating input voltage at 12 the compressor can be driven in a corresponding manner. In one example a 50 Hertz sine wave is supplied at 12 so that the compressor piston will oscillate with motion approximating to simple harmonic motion at 50 Hertz.

65 The supply to the motor 11 is from a d.c. source 13 through a bridge network consisting of four switches and the load in an H configuration.

70 The load 11 is connected in series with an inductor 14 in the crossbar of the H and there is a switch in each of the four arms of the H which consists of a power MOSFET Q in parallel with a diode.

75 It will be appreciated that when the switches Q₁, and Q₄ are closed (and Q₂ and Q₃ are open) current will flow from the d.c. supply 13 through the load 11 in one direction whereas when the switches Q₂ and Q₃ are closed (and Q₁ and Q₄ are open) current will be driven through the load in the other direction, as shown by i₁.

80 If Q₃ is opened, while Q₂ remains closed, current i₂ will flow through the load 11, switch Q₂, and the diode D₄ in a freewheeling path, with energy being neither drawn from the supply 13 nor returned to it; when Q₂ and Q₃ are both open, current i₃ flowing in the load 11 from right to left will flow through the diodes D₁ and D₄ and return energy to the supply.

85 The instantaneous polarity of the input signal at 12 determines whether switches Q₂ and Q₃ are to be used for current to flow from right to left or whether switches Q₁ and Q₄ are to be used for current to flow from left to right. A detector 16 sensitive to the polarity of the input 12 provides one input to each of four AND gates each of which has an output controlling one of the switches Q₁ to Q₄. The output of the detector 16 is also fed to a changeover unit 17 for determining the sense of the error signal in dependence on whether the input waveform 12 is in a positive or a negative half cycle. AND gates G₁ and G₄ have their inputs from the detector 16 connected through invertors so that their outputs will be 0 and their switches off during positive half

cycles of the supply. During those positive half cycles the gates G2 and G3 will receive a 1 input from the detector 16.

A feedback signal proportional to the voltage across the load 11 is supplied at 18 to a comparator 19 for producing an error signal in response to any difference between the instantaneous value of the input voltage at 12 and the load feedback voltage at 18. That error signal after passing through the change-over unit 17 is supplied to a pulse width modulator controller 21 which operates in combination with a modulus unit 22 and a modulator 23 to supply a square wave signal at 24 for switching the switches Q_1 to Q_4 on and off as required. The square wave may be of constant frequency but with mark and space lengths controlled in accordance with the magnitude of the error signal and thus in accordance with the extent to which the load voltage is not tracking the input voltage.

The error signal is also fed to a detector 26 responsive to the sense of the error signal to supply a signal to one input of a NOR gate 27 whose output is connected to one input of each of AND gates G_2 and G_4 . The output at 24 from the pulse width modulator 23 is fed through an inverter to the other input of the NOR gate 27.

The output of the NOR gate 27 is used to control the switches Q_2 and Q_4 in the respective negative and positive half cycles of the input 12 so that the freewheeling circuit such as i_2 or the regenerating circuit such as i_3 will be used in dependence on whether the load voltage is below or above the corresponding instantaneous input voltage.

The output from the detector 26 is also connected to one input of each of the AND gates G_1 and G_3 for ensuring corresponding operation of the switches Q_1 and Q_3 .

The effect is that if the voltage across the load 11 is less than the voltage corresponding to the input 12 so that the error signal is positive, then Q_2 is permanently on and Q_3 is modulated on and off by the pulse width modulated square wave to increase the load voltage. That is for positive half cycles of the input at 12; for negative half cycles it will be Q_4 that is permanently on and Q_1 that is cycled on and off.

On the other hand if the voltage across the load is greater than the voltage equivalent at 12 then Q_3 (or Q_1) is permanently switched off and Q_2 (or Q_4) is alternately switched on and off by the pulse width modulated square wave so that current alternately circulates and is fed back to the d.c. Source 13 so that the load voltage can decay to track the input voltage.

A typical frequency of the pulse width modulated square wave is 20 KHz.

The inductor 14 ensures that current cannot decay instantaneously.

It will be appreciated that a sine wave at

the input 12 is merely one example of an input wave that could be used. If a special pattern of load voltage is required then the system will ensure appropriate control provided the corresponding reference voltage can be generated and applied at 12.

The circuit uses as the feedback signal at 18 the voltage across the load 11 but it would also be possible to use load current as the feedback signal. That would involve a load current-to-voltage converter to provide a signal for the comparator 19.

A control circuit of this kind is of great value with lightly damped load in which the drive is highly dependent on the drive voltage.

In an alternative embodiment shown in Figure 2 the weight and volume of the apparatus can be reduced by eliminating the inductor 14 and replacing it by a capacitor 31 in parallel with the load 11. The four diodes D are omitted.

Operation is generally similar to that described with reference to Figure 1. However, there are only two modes, namely the mode where energy is supplied from the source 13 to the load 11 and the capacitor 31 when the switches Q_1 and Q_4 (or Q_2 and Q_3) are closed, and a decay mode in which the voltage across the capacitor decays through the load 11 when the switch Q_1 (or Q_3) is open. The voltage across the capacitor 31 is used as a feedback signal.

In a further embodiment shown in Figure 3 the load 11 and the switches Q_1 to Q_4 are as in Figure 2, but the bridge is energised from the DC source 13 through a transformer 33 having a semiconductor switch 34 in series with its primary winding and switched in accordance with the output of the pulse width modulator 23. A capacitor 35 is connected in series with a diode 36 across the secondary of the transformer 33 and the capacitor 35 provides the power supply to the bridge and load. A potential divider 37 consisting of two resistors in series connected across the capacitor 35 is used to provide a feedback signal at 38 to the comparator 19.

The sinusoidal (or other) reference input signal at 12 is fed to the comparator 19 through the modulus unit 22 so that the reference signal at the comparator 19 is a full-wave rectified sine wave at X. The reference waveform 12 is also supplied through a zero point detector 39 to control the switches Q_1 to Q_4 through amplifiers 41 to 44, of which amplifiers 42 and 43, controlling switches Q_1 and Q_4 act as inverters. The effect is merely that in positive halfcycles the reference wave 12, Q_1 and Q_4 will be on and Q_2 and Q_3 , off, whereas in the other halfcycles, Q_2 and Q_3 will be on and Q_1 and Q_4 will be off.

The signal at X at the output of the modulus unit 22 which is the reference input to the comparator 19 will be a fullwave rectified sine wave and that will be compared with a feed-

back signal at 38 of similar form derived from the feedback network 37 across the capacitor 35 which is supplying the load 11.

In alternate halfcycles the load 11 will be supplied from the capacitor 35 in one sense and in the other halfcycles it will be supplied in the other sense and, as with the embodiments of Figures 1 and 2 the feedback signal at 38 is proportional to the voltage across the load 11 and that ensures effective tracking of the input wave at 12.

The circuit does not have the complicated switching arrangement of Figures 1 and 2 and the transformer 33 being a high frequency transformer, is small, light and cheap. For operation at 100 kHz it might be a 1 inch cube.

It should be noted that in each of the embodiments of Figures 2 and 3 the capacitor 31 or 35 needs to be carefully chosen with reference to the load characteristics of the desired load waveform. Thus, considering Figure 3, for example, it will be appreciated that during the period of each of the rectified halfcycles of the waveform when the slope of the waveform is negative, as much as possible, and preferably all, of the energy stored in the capacitor 35 plus any added energy required to maintain the wave shape should be dissipated by the load if a discontinuity is not to occur as the bridge switches over for the next halfcycle.

CLAIMS

1. A switching bridge circuit for driving a load from a d.c. supply in which the bridge includes switches controlled in accordance with a desired input wave form.

2. A switching bridge circuit for driving a load from a d.c. supply with the switches in the bridge being controlled in accordance with a desired input wave form, in which a function of the load current or voltage is fed back and compared with the input wave form and a resulting error signal is used to control the switches, logic means being arranged to operate the switches so that when the error signal has one polarity energy is fed from the load to the supply and when the error signal has the other polarity energy is drawn to the load from the supply.

3. A bridge circuit as claimed in either of the preceding claims which is arranged to have a mode of operation in which current in the load free wheels in the bridge circuit without drawing energy from the supply or supplying energy to the supply.

4. A bridge circuit as claimed in any of the preceding claims including logic means responsive to the polarity of the input wave form and arranged to ensure that the appropriate pair of diagonally opposite switches are used to control the load current or voltage in the respective positive and negative portions of the input wave form.

5. A bridge circuit as claimed in any of the

preceding claims including a pulse width modulator arranged to control the switches in the bridge circuit.

6. A bridge circuit as claimed in any of Claims 2 to 5 including logic means arranged in response to the sense of the error signal to control the operation of a diagonal pair of switches so that the load current alternately free wheels and flows to the d.c. supply.

7. A bridge circuit as claimed in Claim 6 in which when the required load output is greater than the actual load output current is supplied to the d.c. supply whereas when the required load output is less than the actual load output current is drawn through the load from the supply.

8. A switching bridge circuit constructed and arranged substantially as herein specifically described with reference to Figure 1, Figure 2 or Figure 3 of the accompanying drawings.

9. A switching bridge circuit for driving a load from a d.c. supply including means for supplying a reference signal defining a desired load wave form and feedback means for feeding back to a control circuit a signal derived from the current in, or voltage across, the load.

CLAIMS

Amendments to the claims have been filed, and have the following effect:

Claims 1—9 above have been deleted.

New claims have been filed as follows:

1. A switching bridge circuit for driving a load from a DC supply, the circuit comprising a capacitor arranged to be connected in parallel with the load, a function of the load current or voltage being arranged to be compared with an externally applied waveform, and the resulting error signal being used to control switches which control the rate of energy transfer to the load.

2. A bridge circuit as claimed in claim 1 in which energy is transferred to the load via a switching transformer arranged to charge the capacitor.

3. A bridge circuit as claimed in claim 2 in which the capacitor is connected in series with a diode across a secondary winding of the transformer.

4. A bridge circuit as claimed in claim 2 or claim 3 in which the error signal is arranged to vary the duty cycle of the transformer.

5. A bridge circuit as claimed in any one of claims 2 to 4 in which the function of the load current or voltage is derived from a signal part way along a potential divider in parallel with the capacitor.

6. A switching bridge circuit for driving a load from a DC supply, the circuit comprising an inductor arranged to be connected in series with the load, a function of the load current or voltage being arranged to be compared with an externally applied waveform, and the result-

ing error signal being used to control switches which control the rate of energy transfer to the load.

7. A bridge circuit as claimed in claim 6 including logic means arranged to operate the switches so that when the error signal has one polarity energy is fed from the load to the supply and when the error signal has the other polarity energy is drawn from the load to the supply.

8. A bridge circuit as claimed in claim 7 in which the logic means are arranged to operate in response to the polarity of the error signal to control the operation of a diagonal pair of switches so that the load current alternately free wheels and flows to the DC supply.

9. A bridge circuit as claimed in claim 8 in which when the required load output is greater than the actual load output current is supplied to the DC supply whereas when the required load output is less than the actual load output current is drawn through the load from the supply.

10. A bridge circuit as claimed in any one of the preceding claims including means responsive to the polarity of the input waveform and arranged to ensure that the appropriate pair of diagonally opposite switches are used to control the load current or voltage in the respective positive and negative portions of the input waveform.

11. A bridge circuit as claimed in any one of the preceding claims in which the switches are arranged to be controlled by a duty cycle modulator.

12. A bridge circuit as claimed in any one of the preceding claims which is arranged to have a mode of operation in which the current in the load free wheels in the bridge circuit without drawing energy from the supply or supplying energy to the supply.

13. A switching bridge circuit for driving a load from a DC supply, the load being arranged for connection in the crossbar of the bridge and a controllable switch located in each of the arms of the bridge, a function of the load current or voltage being arranged to be compared with an externally applied waveform and the resulting error signal being used to control the switches, thereby controlling energy transfer to the load.

14. A switching bridge circuit constructed and arranged substantially as specifically described with reference to figure 1.

15. A switching bridge circuit constructed and arranged substantially as specifically described with reference to figure 2.

16. A switching bridge circuit constructed and arranged substantially as specifically described with reference to figure 3.